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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.



Final Rejection

The office action is in response to applicants amendment of 11 February 2008.

Claims 1-20 are pending in this application.

The objection to the disclosure has been withdrawn.

The objection to claim 20 has been withdrawn.

The 35 U.S.C. 101 rejections are being maintained at the moment.

Response to amendment

Applicants arguments have been fully considered, and are only found persuasive to the extent that new references Sakalian et al. (U.S. Patent No. 5,056,119) teaches "selecting a first portion from a plurality of possible positions" and also "if the first selected position is not correct, selecting a second position from a second plurality of possible positions" (column 1, line 16 – column 2, line 7). Further, new reference O' Connor et al. (U.S. Patent No. 5,005,191) teaches "each of the second plurality of possible positions comprises each of the first plurality of possible positions shifted by one position unit" (column 2, lines 26 – 42) and (column 3, lines 52 – 66).

Response to applicants remarks

On page 8, the applicant mentions there is no disclosure in Kerns, however, of "selecting a first portion from a first plurality of possible positions", as is recited in part, in claim 1. Kern also fails to disclose "if the first selected position is not correct, selecting a second position from a second plurality of possible position" as is recited in part, in claim 1.

The Examiner agrees with the statement, however points out that new reference Sakalian et al. (U.S. Patent No. 5,056,119) teaches "selecting a first portion from a plurality of possible positions" and also "if the first selected position is not correct, selecting a second position from a second plurality of possible positions" (column 1, line 16 – column 2, line 7).

On page 8, the applicant mentions Wright also fails to teach or suggest "each of the second plurality of possible positions comprises each of the first plurality of possible positions shifted by one position unit."

The Examiner agrees with the statement, however points out that new reference O' Connor et al. (U.S. Patent No. 5,005,191) teaches "each of the second plurality of possible positions comprises each of the first plurality of possible positions shifted by one position unit" (column 2, lines 26 – 42) and (column 3, lines 52 – 66).

35 U.S.C. 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1 – 3, 8 – 9 and 20 are rejected under 35 U.S.C. 101 as being non-statutory for failing to produce any real world tangible result.

35 U.S.C. 103 Rejection

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 – 3, 8-9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kerns et al. (U.S. Patent No. 6,819,679), Sakalian et al. (U.S. Patent No. 5,056,119) in view of O' Connor et al. (U.S. Patent No. 5,005,191).

With respect to claim 1, the Kerns et al. reference teaches testing the first selected position (column 5, lines 61 – 66), (column 6, lines 19 – 23). The Kerns et al. reference does not teach selecting a first position from a plurality of possible positions; if

the first selected positions is not correct, selecting a second position from a second plurality of possible positions and wherein each of the second plurality of possible positions comprises each of the first plurality of possible positions shifted by one position unit wherein the selected second position is used to determine the position of the synchronization pattern in the serial stream of incoming data.. The Sakalian et al. reference teaches selecting a first position from a plurality of possible positions and if the first selected positions is not correct, selecting a second position from a second plurality of possible positions (column 1, line 16 – column 2, line 7). The O' Connor et al. reference teaches and wherein each of the second plurality of possible positions comprises each of the first plurality of possible positions shifted by one position unit wherein the selected second position is used to determine the position of the synchronization pattern in the serial stream of incoming data (column 2, lines 26 – 42) and (column 3, lines 52 – 66). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Kerns et al. and Sakalian et al. to incorporate selecting a first position from a plurality of possible positions and if the first selected positions is not correct, selecting a second position from a second plurality of possible positions into the claimed invention. The motivation for selecting a first position from a plurality of possible positions and if the first selected positions is not correct, selecting a second position from a second plurality of possible positions is to establish quick synchronization and that the circuit not be fooled into believing that synchronization has been lost merely because a certain number of bits are received in a condition that accurate detection as to their logic value cannot be made (column 1, lines 8-14 – Sakalian et al. reference). Thus it would also have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined

the references Kerns et al. and O'Connor et al. to incorporate wherein each of the second plurality of possible positions comprises each of the first plurality of possible positions shifted by one position unit wherein the selected second position is used to determine the position of the synchronization pattern in the serial stream of incoming data into the claimed invention. The motivation for wherein each of the second plurality of possible positions comprises each of the first plurality of possible positions shifted by one position unit wherein the selected second position is used to determine the position of the synchronization pattern in the serial stream of incoming data is because it would be desirable to provide a synchronization circuit for a serial data receiver which has improved response, and which is simply and easily designed into a portion of an integrated circuit (column 2, lines 55-58 - O'Connor et al. reference).

With respect to claim 2, the Kerns et al. reference teaches testing the second selected position (column 6, lines 37-42); if the second selected position is not correct, selecting a third position from the first plurality of possible positions (column 6, lines 37-42), (see Fig.9, Locate next frame – 505);

With respect to claim 3, the Kerns et al. and Wright et al. references teach all of the limitations of claim 1. The kerns et al. reference does not teach rotating a segment of the serial stream of data so that the synchronization pattern is at a predetermined position. The Wright et al. reference teaches rotating a segment of the serial stream of data so that the synchronization pattern is at a predetermined position (column 5, lines 54 – column 6, line 2), (column 3, lines 42-52). Thus it would have been obvious to have combined the references Kerns et al. and Wright et al. to have incorporated rotating a

segment of the serial stream of data so that the synchronization pattern is at a predetermined position. The motivation for rotating a segment of the serial stream of data so that the synchronization pattern is at a predetermined position is so the output signal is aligned with the boundary of a byte of the data stream.

With respect to claim 8, the Kerns et al. reference teaches wherein the step of selecting includes determining a subset of the first plurality of possible positions as a function of a segment of the serial stream of data (column 4, lines 37-54), column 1, lines 46-65).

With respect to claim 9, the kerns et al. reference teaches wherein the step of selecting includes determining a subset of the first plurality of possible positions as a function of a previous selection (column 6, lines 19-23).

With respect to claim 18, the Kerns et al. reference teaches wherein the serial stream of data comprises a plurality of frames, each frame comprising a data field and a synchronization pattern (see Fig. 5, Load frames N and N+1 – 202).

Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kerns et al. (U.S. Patent No. 6,819,679), Sakalian et al. (U.S. Patent No. 5,056,119), O'Connor et al. (U.S. Patent No. 5,005,191) in view of Wright et al. (U.S. Patent No. 7,103,049).

With respect to claim 4, all of the limitations of claim 1 have been addressed. The Kerns et. al reference does not teach selecting a portion of the rotated segment; selecting a portion of a previous rotated segment and combining the selected portions to form an output segment of the serial stream of data, wherein the output segment is longer than the segment. The Wright et al. reference teaches selecting a portion of the rotated segment (column 6, line 61 – column 7, line 5); selecting a portion of a previous rotated segment (column 2, lines 9-24), (column 2, lines 38-45); combining the selected portions to form an output segment of the serial stream of data, wherein the output segment is no longer than the rotated segment (column 2, lines 9-24). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Kerns et al. and Wright et al. to incorporate selecting a portion of the rotated segment; selecting a portion of a previous rotated segment and combining the selected portions to form an output segment of the serial stream of data, wherein the output segment is longer than the segment into the claimed invention. The motivation for selecting a portion of the rotated segment; selecting a portion of a previous rotated segment and combining the selected portions to form an output segment of the serial stream of data, wherein the output segment is longer than the segment is the ability to conduct high speed data communications between remotely separated data processing systems and associated subsystems (column 1, lines 16-18 – Wright et al. reference).

With respect to claim 5, all of the limitations of claim 4 have been addressed. The Kerns et. al reference does not teach wherein the output segment of the serial stream of data comprises synchronization patterns at fixed positions. The Wright et al. reference

teaches wherein the output segment of the serial stream of data comprises synchronization patterns at fixed positions (column 2, lines 9-24). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Kerns et al. and Wright et al. to incorporate wherein the output segment of the serial stream of data comprises synchronization patterns at fixed positions into the claimed invention. The motivation for wherein the output segment of the serial stream of data comprises synchronization patterns at fixed positions is the ability to conduct high speed data communications between remotely separated data processing systems and associated subsystems (column 1, lines 16-18 – Wright et al. reference).

With respect to claim 6, all of the limitations of claim 4 have been addressed. The Kerns et. al reference does not teach incrementing a first counter if the output segment contains a synchronization pattern at a predetermined position. The Wright et al. reference teaches incrementing a first counter if the output segment contains a synchronization pattern at a predetermined position (column 2, lines 9-24); incrementing a second counter if the output segment does not contain a synchronization pattern at the predetermined position (column 2, lines 46-56). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Kerns et al. and Wright et al. to incorporate incrementing a first counter if the output segment contains a synchronization pattern at a predetermined position into the claimed invention. The motivation for incrementing a first counter if the output segment contains a synchronization pattern at a predetermined position is the ability to conduct

high speed data communications between remotely separated data processing systems and associated subsystems (column 1, lines 16-18 – Wright et al. reference).

With respect to claim 7, all of the limitations of claim 6 have been addressed. The Kerns et. al reference does not teach determining a state of synchronization as a function of the first and second counters. The Wright et al. reference teaches determining a state of synchronization as a function of the first and second counters (column 2, lines 46-56), (column 3, lines 11-41). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Kerns et al. and Wright et al. to incorporate determining a state of synchronization as a function of the first and second counters. The Wright et al. reference teaches determining a state of synchronization as a function of the first and second counters into the claimed invention. The motivation for determining a state of synchronization as a function of the first and second counters. The Wright et al. reference teaches determining a state of synchronization as a function of the first and second counters is the ability to conduct high speed data communications between remotely separated data processing systems and associated subsystems (column 1, lines 16-18 – Wright et al. reference).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kerns et al. (U.S. Patent No. 6,819,679), Sakalian et al. (U.S. Patent No. 5,056,119), O' Connor et al. (U.S. Patent No. 5,005,191) in view of Mo et al. (U.S. Patent No. 7,151,773).

With respect to claim 19, the Kerns et al. reference teaches synchronization pattern comprises two bits column 4, lines 19-53). The Kerns et al. reference does not teach wherein the data field comprises 64 bits. The Mo et al. reference teaches wherein the data field comprises 64 bits (column 9, lines 31-48). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Kerns et al. and Mo et al. to incorporate wherein the data field comprises 64 bits. The Mo et al. reference teaches wherein the data field comprises 64 bits into the claimed invention. The motivation for wherein the data field comprises 64 bits. The Mo et al. reference teaches wherein the data field comprises 64 bits is to provide an advantage over connection oriented networks in terms of simplicity, reliability and scalability (column 1, lines 45 – 46 – Mo et al. reference).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kerns et al. (U.S. Patent No. 6,819,679), Sakalian et al. (U.S. Patent No. 5,056,119), O' Connor et al. (U.S. Patent No. 5,005,191) in view of Taborek, Sr. et al. (U.S. 7,020,729).

With respect to claim 20, all of the limitations of claim 1 have been addressed. The Kerns et al. reference does not teach wherein the serial stream of data is 10 Gb Ethernet data. The Taborek, Sr. et al. reference teaches that serialized data can be a 10 Gb Ethernet data (column 2, line 55 – column 3, line 16). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Kerns et al. and Taborek, Sr. et al. to incorporate wherein the

serial stream of data is 10 Gb Ethernet data into the claimed invention. The motivation for wherein the serial stream of data is 10 Gb Ethernet data is for better error detection and fault isolation capabilities (column 3, lines 66-67 - Taborek, Sr. et al. reference).

Claims 10,13-16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taborek, Sr. et al. (U.S. 7,020,729) further in view of Wright et al. (U.S. Patent No. 7,103,049)

With respect to claim 10, the Taborek, Sr. et al. reference teaches a serial to parallel converter for converting the serialized framed data to a parallel framed data (column 3, lines 17-25); a guesser for guessing a position of a frame boundary in the parallel framed data (column 5, line 61 – column 6, line 6); a tester for testing the data output to determine if the frame boundary is at a predetermined position in the data output (column 6, lines 6 – 21); counting mechanism for counting when the frame boundary is at the predetermined position in the data output (column 1, lines 13 – 31); a state machine, the state machine determining if the device is in a state of synchronization based on the counting mechanism (column 5, lines 25-33). The Taborek, Sr. et al. reference does not teach a rotator for rotating the parallel framed data in accordance with the position guessed by the guesser and a selector for selecting a portion of the rotated parallel framed data and a portion of the delayed version of the rotated parallel framed data to form a data output. The Wright et al. reference teaches a rotator for rotating the parallel framed data in accordance with the position guessed by the guesser (column 2, lines 57 – column 3, line 10), (column 3, lines 42-52); a selector for selecting a portion of the rotated parallel framed data and a portion of the delayed

version of the rotated parallel framed data to form a data output (column 6, line 61 – column 7, line 5), (column 5, lines 28-40) and 9column 6, lines 17-35). Thus it would have been obvious to combine the references Taborek et al. and Wright et al. to incorporate a rotator for rotating the parallel framed data in accordance with the position guessed by the guesser and a selector for selecting a portion of the rotated parallel framed data and a portion of the delayed version of the rotated parallel framed data to form a data output into the claimed invention. The motivation for a rotator for rotating the parallel framed data in accordance with the position guessed by the guesser and a selector for selecting a portion of the rotated parallel framed data and a portion of the delayed version of the rotated parallel framed data to form a data output is so that the synchronization pattern is at a predetermined position is so the output signal is aligned with the boundary of a byte of the data stream.

With respect to claim 13, all of the limitations of claim 10 have been addressed above. The Taborek, Sr. et al. reference does not teach a shifter for shifting the parallel framed data by an odd number of bits and a selector for selecting the parallel framed data or the parallel framed data shifted by the odd number of bits, wherein the selected data is provided to the rotator. The Wright et al reference teaches a shifter for shifting the parallel framed data by an odd number of bits (column 2, lines 38-45). The Wright et al. reference teaches a selector for selecting the parallel framed data or the parallel framed data shifted by the odd number of bits, wherein the selected data is provided to the rotator (column 2, line 38). Thus it would have been obvious to have combine the references Taborek, Sr. et al. and Wright et al. to have incorporated a shifter for shifting the parallel framed data by an odd number of bits. The motivation for a shifter for shifting

the parallel framed data by an odd number of bits is so cell delineation can be achieved. (column 3, lines 50-51 – Wright et al. reference).

With respect to claim 14, all of the limitations of claim 13 have been addressed. The Taborek, Sr. et al. reference does not teach wherein the odd number of bits is one. The Wright et al. reference teaches wherein the odd number of bits is one (column 2, lines 46-56). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Taborek, Sr. et al. reference and Wright et al. to incorporate wherein the odd number of bits is one into the claimed invention. The motivation for wherein the odd number of bits is one is so cell delineation can be achieved. (column 3, lines 50-51 – Wright et al. reference).

With respect to claim 15, the Taborek, Sr. et al. reference teaches wherein the serialized framed data comprises a plurality of frames, each frame comprising a data field and a synchronization pattern (column 8, lines 46-55).

With respect to claim 16, the Taborek, Sr. et al. reference teaches wherein the data field comprises 64b/66b (column 9, lines 10-27). The Taborek, Sr. et al. and Wright et al. references also addresses various aspects of ethernet technology that address field, synchronization, transmission and other aspects that make data field segmentation obvious to one skilled in the art.

With respect to claim 17, the Taborek, Sr. et al. reference teaches wherein the serialized data is a 10 Gb Ethernet data (column 2, line 55 – column 3, line 16).

Claims 11-12 are rejected under Taborek, Sr. et al. (U.S. 7,020,729), Wright et al. (U.S. Patent No. 7,103,049) further in view of Swoboda et al. (U.S. Patent No. 6,085,336).

With respect to claim 11, all of the limitations of claim 10 have been addressed. The Taborek, Sr. et al. reference does not teach an exhaust register, the exhaust register storing one or more positions guessed by the guesser determined not to contain a frame boundary. The Swoboda et al. reference teaches exhaust register storing one or more positions guessed by the guesser determined not to contain a frame boundary (column 38, lines 32-41). Thus it would have been obvious to have combined the references Taborek, Sr. et al. and Swoboda et al. references to incorporate an exhaust register storing one or more positions guessed by the guesser determined not to contain a frame boundary. The motivation for an exhaust register storing one or more positions guessed by the guesser determined not to contain a frame boundary is to provide improved emulation, simulation and testability architectures and methods that are viable alternative to high capital-cost test equipment and systems (column 3, lines 25-27 – Swoboda et al. reference).

With respect to claim 12, all of the limitations of claim 11 have been addressed. The Taborek, Sr. et al. reference does not teach wherein the guesser excludes the one or more positions stored in the exhaust register as possible positions of the frame

boundary. The Swoboda et al. reference teaches wherein the guesser excludes the one or more positions stored in the exhaust register as possible positions of the frame boundary (column 38, lines 58-65). Thus it would have been obvious to have combined the references Taborek, Sr. et al. and Swoboda et al. references to incorporate wherein the guesser excludes the one or more positions stored in the exhaust register as possible positions of the frame boundary into the claimed invention. The motivation for wherein the guesser excludes the one or more positions stored in the exhaust register as possible positions of the frame boundary is to provide improved emulation, simulation and testability architectures and methods that are viable alternative to high capital-cost test equipment and systems (column 3, lines 25-27 – Swoboda et al. reference).

### Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

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CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Enam Ahmed whose telephone number is 571-270-1729. The examiner can normally be reached on Mon-Fri from 8:30 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached on 571-272-6962.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EA

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/JACQUES H LOUIS-JACQUES/

Supervisory Patent Examiner, Art Unit 2112